

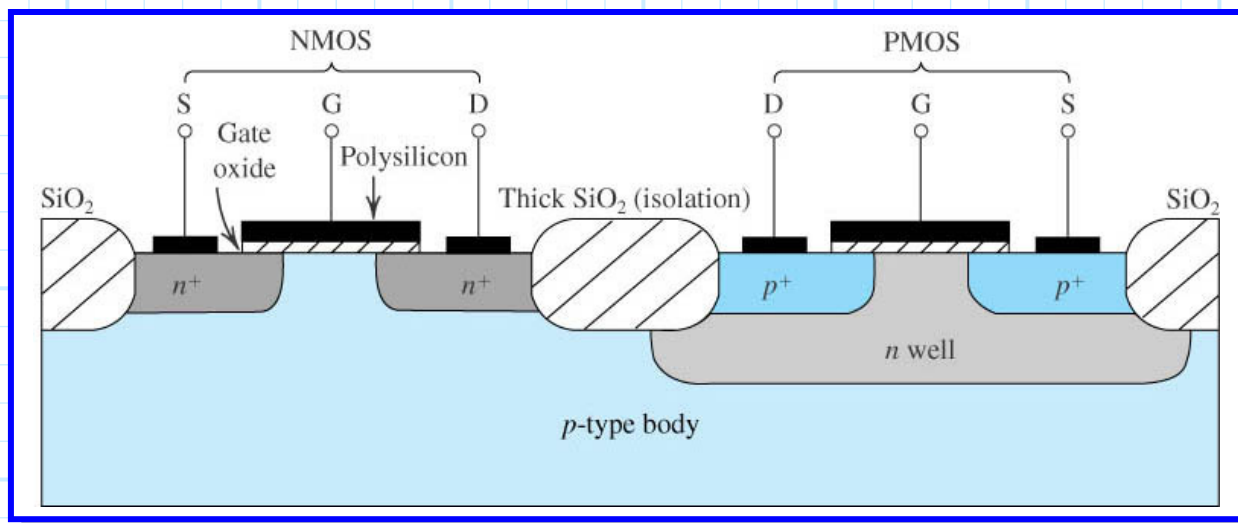
# PMOS and CMOS

In addition to an  $n$ -channel MOSFET device (i.e., NMOS), we can build  $p$ -channel MOSFET (i.e., PMOS) device.

The structure of a PMOS device is essentially the same as an NMOS transistor, except that wherever there was  $n$ -type Silicon there is now  $p$ -type Silicon—and wherever there was  $p$ -type Silicon there is now  $n$ -type Silicon!

Specifically, the PMOS channel is part of a  $n$ -type substrate lying between two heavily doped  $p^+$  wells beneath the source and drain electrodes.

Generally speaking, a PMOS transistor is only constructed in consort with an NMOS transistor. This “pair” of NMOS and PMOS transistors is known as Complementary MOSFETs—**CMOS** for short!

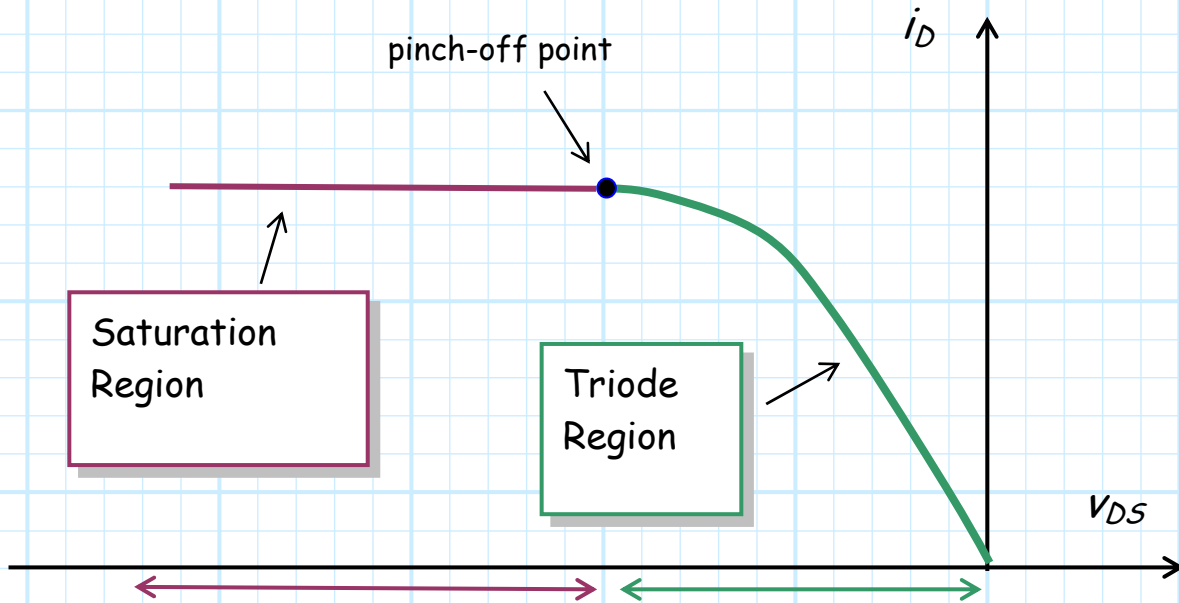


The operation of a PMOS transistor is in many ways **similar** to that of the NMOS device, but in many ways they are also **quite different!**

For example, for a **PMOS** device we find:

- \* To create an inversion layer in the ***n*-type** substrate, we must attract **holes** to the gate electrode.
- \* As a result, a ***p*-type** channel will be induced, connecting the **p+** wells at the drain and the source.
- \* However, to attract **holes** toward the gate, the voltage  $v_{GS}$  must be sufficiently **negative!** The threshold voltage  $V_t$  is thus a **negative** value, so that a channel is induced only if  $v_{GS} < V_t$  (i.e.,  $v_{GS}$  is more **negative** than  $V_t^I$ ).
- \* As a result, a channel is induced in a **PMOS** device **only** if the excess gate voltage  $v_{GS} - V_t$  is **negative** (i.e.,  $v_{GS} - V_t < 0$ ).
- \* Likewise, we find that we typically get current to flow through this channel by making the voltage  $v_{DS}$  **negative**. If we make the voltage  $v_{DS}$  sufficiently **negative**, the ***p*-type** induced channel will **pinch off**.
- \* Note that when  $v_{DS}$  is **negative**, the drain current will flow **from** the PMOS source, to the PMOS drain (i.e., exactly **opposite** that of the NMOS device with a positive  $v_{DS}$ ).

\* Thus, for a **PMOS** device, we **define** current flowing from source to drain as **positive current** (i.e., exactly **opposite** that of the NMOS device).



The **PMOS**  $i_D$  vs.  $V_{DS}$  Curve